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[0001] # DIGITAL BASEBAND RECEIVER INCLUDING A TIME DOMAIN COMPENSATION MODULE FOR SUPPRESSING GROUP DELAY VARIATION DISTORTION INCURRED DUE TO ANALOG LOW PASS FILTER DEFICIENCIES

[0002] ## CROSS REFERENCE TO RELATED APPLICATION

[0003] This application claims priority from U.S. Provisional Patent Application Serial No. 60/482,832, filed June 25, 2003, which is incorporated by reference as if fully set forth herein.

[0004] ## FIELD OF THE INVENTION

[0005] The present invention generally relates to receiver design in wireless communication systems. More particularly, the present invention relates to digital signal processing (DSP) techniques used to compensate for group delay variation distortion introduced in an analog radio receiver.

[0006] ## BACKGROUND

[0007] Existing wireless system architectural configurations impose stringent constraints on the system designer with regards to receiving communication signals. Moreover, such configurations often provide low reliability communication links, high operating costs, and an undesirably low level of integration with other system components.

[0008] As shown in Figure 1, a conventional RF receiver 100 includes an analog radio receiver 105, at least one analog to digital converter (ADC) 110, a controller 115 and a modem 120. The analog radio receiver 105 is a direct conversion (DC) receiver which includes an antenna 125 for receiving a wireless communication signal, a bandpass filter 130, a low noise amplifier (LNA) 135, an optional second filter 140 (e.g., bandpass filter), a demodulator 145 having two outputs 150, 155, a phase-locked loop

(PLL) 160 and first and second analog low pass filters (LPFs) 165, 170 for controlling bandwidth selectivity.

[0009] The modem 120 controls the switching of the LNA 135. The PLL 160 generates a local oscillator (LO) signal to control the two outputs 150, 155 of the demodulator 145. The output 150 is an in-phase (I) output of the demodulator 145 for outputting a real signal component of the wireless communication signal. The output 155 is a quadrature (Q) output of the demodulator 145 for outputting an imaginary signal component of the wireless communication signal.

[0010] In the conventional RF receiver 100 of Figure 1, the ADC 110 is connected to the real and imaginary signal outputs 150, 155, via the analog LPFs 165, 170, respectively. An analog real signal component 175 is output from the LPF 165 to a real input port of the ADC 110 and an analog imaginary signal component 180 is output from LPF 170 to an imaginary input port of the ADC 110. The ADC 110 outputs digital real and imaginary signal outputs 185, 190. The controller 115 maintains control over all of the active components of analog radio receiver 105 and the ADC 110.

[0011] In the analog radio receiver 105, the analog LPFs 165, 170, are utilized to guarantee the spectral shape of the wireless communication signal received via the antenna 125 before being sampled at the ADC 110. Typically, the specifications (e.g., error vector magnitude) on the analog LPFs 165, 170, are very stringent such that the implementation requires high order filtering. Implementing high order filter designs for the analog LPFs 165, 170, may be complicated and expensive. Thus, the tolerances on parts for the analog LPFs 165, 170 may lead to unacceptable production yield. Reducing the design complexity of the analog LPFs 165, 170, may be accomplished with a lower order filter design with less stringent specifications. However, using such a filter design in the analog LPFs 165, 170, will result in the occurrence of a group delay variation distortion if no compensation is introduced after the analog LPFs 165, 170.

[0012] Because the costs of LPFs that process RF analog signals are higher than the components that use DSP, it is desired to provide a digital baseband (DBB) system, including a low cost receiver with low noise and minimal power requirements, which utilizes DSP techniques to compensate for group delay variation distortion caused by analog LPFs.

[0013] SUMMARY

[0014] The present invention is a DBB transmitter for receiving and processing a wireless communication signal. The DBB receiver includes a demodulator, first and second analog LPFs, first and second digital gain control circuits, and a digital time domain compensation module which removes group delay variation distortion, introduced by the first and second analog LPFs, from real and imaginary signal components of the communication signal.

[0015] The present invention may be incorporated into a DBB transmitter, a wireless transmit/receive unit (WTRU), an integrated circuit (IC), a wireless communication system and method, or any other desired communication mechanism.

[0016] The demodulator outputs analog real and imaginary signal components in response to receiving the communication signal. The first analog low pass filter (LPF) receives the analog real signal component from the demodulator and outputs a distorted analog real signal component. The second analog LPF receives the analog imaginary signal component from the demodulator and outputs a distorted analog imaginary signal component. The first digital gain control circuit receives the distorted analog real signal component from the first analog LPF and outputs a processed distorted digital real signal component. The second digital gain control circuit receives the distorted analog imaginary signal component from the second analog LPF and outputs a processed distorted digital imaginary signal component. The digital time domain compensation module receives the processed distorted digital real and

imaginary signal components and outputs digital real and imaginary compensated signal components.

[0017] The digital time domain compensation module may include a real signal path, a plurality of real signal component delay units connected in series along the real signal path, a plurality of real filter coefficient positions, a first combiner having a plurality of inputs, and a plurality of active real filter coefficient units located at a subset of the real filter coefficient positions. Each of the active real filter coefficient units may have an input connected to the real signal path and an output connected to one of the inputs of the first combiner. The first combiner may output the real compensated signal component.

[0018] The digital time domain compensation module may further include an imaginary signal path, a plurality of imaginary signal component delay units connected in series along the imaginary signal path, a plurality of imaginary filter coefficient positions, a second combiner having a plurality of inputs, and a plurality of active imaginary filter coefficient units located at a subset of the imaginary filter coefficient positions. Each of the active imaginary filter coefficient units may have an input connected to the imaginary signal path and an output connected to one of the inputs of the second combiner. Thee second combiner may output the imaginary compensated signal component.

[0019] The digital time domain compensation module may includes a plurality of real filter coefficient unit positions and a plurality of imaginary filter coefficient unit positions. A plurality of active real filter coefficient units may be present at a subset of the real filter coefficient unit positions and a plurality of active imaginary filter coefficient units may be present at a subset of the imaginary filter coefficient unit positions.

[0020] The digital time domain compensation module may further include a plurality of real signal component delay units and a plurality of imaginary signal

component delay units having inputs and outputs connected to the inputs of respective ones of the active filter coefficient units.

[0021] The digital time domain compensation module may be a finite impulse response (FIR) filter having characteristics which are selected such that the frequency domain response of the digital time domain compensation module is the inverse of the frequency domain response of the analog LPFs.

[0022] The first digital gain control circuit may include a logarithmic amplifier, an analog to digital converter (ADC), and a look up table (LUT). The logarithmic amplifier may compress the distorted analog real signal component from a wider dynamic range to a lower dynamic range. The ADC may convert the compressed distorted analog real signal component to a compressed distorted digital real signal component. The LUT may provide an anti-log function used to decompress the compressed distorted digital real signal component.

[0023] The second digital gain control circuit may include a logarithmic amplifier, an ADC, and an LUT. The logarithmic amplifier may compress the distorted analog imaginary signal component from a wider dynamic range to a lower dynamic range. The ADC may convert the compressed distorted analog imaginary signal component to a compressed distorted digital real signal component. The LUT may provide an anti-log function used to decompress the compressed distorted digital imaginary signal component.

[0024] BRIEF DESCRIPTION OF THE DRAWING(S)

[0025] A more detailed understanding of the invention may be had from the following description of a preferred example, given by way of example and to be understood in conjunction with the accompanying drawing wherein:

[0026] Figure 1 is a block diagram of a conventional RF receiver including an analog radio receiver;

[0027] Figure 2 is a block diagram of a DBB RF receiver configured in accordance

with a preferred embodiment of the present invention; and

[0028] Figure 3 shows an exemplary configuration of the digital time domain compensation module in the DBB RF receiver of Figure 2.

[0029] DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0030] Figure 2 is a block diagram of a DBB RF receiver 200, configured in accordance with a preferred embodiment of the present invention. Although the invention will be referred to in terms of being implemented upon a receiver 200, it should also be understood by those of skill in the art that the invention pertains equally to a transceiver.

[0031] Preferably, the method and system disclosed herein is incorporated into a wireless transmit/receive unit (WTRU). Hereafter, a WTRU includes but is not limited to a user equipment, mobile station, fixed or mobile subscriber unit, pager, or any other type of device capable of operating in a wireless environment. The features of the present invention may be incorporated into an integrated circuit (IC) or be configured in a circuit comprising a multitude of interconnecting components.

[0032] The present invention is applicable to communication systems using time division duplex (TDD), time division multiple access (TDMA), frequency division duplex (FDD), code division multiple access (CDMA), CDMA 2000, time division synchronous CDMA (TDSCDMA), and orthogonal frequency division multiplexing (OFDM). However, the present invention is envisaged to be applicable to other types of communication systems as well.

[0033] As shown in Figure 2, the DBB RF receiver 200 includes an analog radio receiver 105, a real signal path digital gain control circuit 205A, an imaginary signal path digital gain control circuit 205B, and a digital time domain compensation module 210. The digital time domain compensation module 210 has a real signal input 240 connected to the analog real signal component 175 via the real signal path digital gain control circuit 205A. The digital time domain compensation module 210 also has an

imaginary signal input 250 connected to the analog imaginary signal component 180 via the imaginary signal path digital gain control circuit 205B. The digital time domain compensation module 210 further includes real and imaginary compensated signal outputs 260, 270. The digital time domain compensation module 210 and the digital gain control circuits 205A, 205B, may be controlled by the controller 115.

[0034] Still referring to Figure 2, each of digital gain control circuits 205A, 205B, include a logarithmic amplifier 215A, 215B, or other amplifier with known compression characteristics for compressing the input analog signals received from analog radio receiver 105 from a wider dynamic range to a lower dynamic range. In other words, the logarithmic amplifiers 215A, 215B, apply a particular level of amplification to the analog real (I) and imaginary (Q) signal components 175, 180, in accordance with their amplitude. Each of the digital gain control circuits 205A, 205B, further includes an ADC 220A, 220B, a look up table (LUT) 225A, 225B, and a combiner 230A, 230B. The LUTs 225A, 225B, provide an anti-log function used to decompress the converted digital signals based on previously captured compression curve data. The ADCs 220A, 220B, digitize the outputs of logarithmic amplifiers 215A, 215B, and provide the digitized outputs to the LUTs or anti-log functions 225A, 225B, in order to decipher the digital domain of the analog real and imaginary signal components 175, 180. The outputs of the ADCs 220A, 220B, are converted to a linear scale by generating (2*n-1) bit signals. It may be necessary to add one or more additional gain stages before each logarithmic amplifier 215A, 215B, if the existing gain is not sufficient to promote saturation. The combiners 230A, 230B, combine the digitized outputs of the LUTs 225A, 225B, with sign bits 235A, 235B, provided by saturated outputs of the logarithmic amplifiers 215A, 215B, to generate a digital real signal component 240 and a digital imaginary signal component 250. The sign bits 235A, 235B, are created from saturated outputs of logarithmic amplifiers 215A, 215B, respectively.

[0035] The digital gain control circuits 205A, 205B, are used to compensate for channel loss variation and to support a large dynamic range of incoming signals (e.g.,

from 100 dBm to -20 dBm). The digital gain control circuits 205A, 205B, are also used to minimize the number of bits required for operating the ADCs 220A, 220B, and are designed to efficiently compensate for channel loss variation in an expeditious manner, without distorting the signal envelope. The digital gain control circuits 205A, 205B, have a linear response, in dB-per-volt. In a closed loop system, the digital gain control circuits 205A, 205B, are used to maintain functions such as stability, settling time, overshoot, etc.

[0036] Figure 3 shows an exemplary configuration of the digital time domain compensation module 210 in the DBB RF receiver 200. The digital time domain compensation module 210 is used to suppress the distortion introduced by the analog LPFs 165, 170, on the real and imaginary analog outputs 150, 155, of the demodulator 145. The digital time domain compensation module 210 may be a digital finite impulse response filter (FIR) having characteristics which are selected such that the frequency domain response of the digital time domain compensation module 210 is the inverse of the frequency domain response of the analog LPFs 165, 170, in the analog radio receiver 105. When the frequency response of the digital time domain compensation module 210 is convolved with the frequency response of the analog LPFs 165, 170, the distortion caused by the analog LPFs 165, 170, is suppressed.

[0037] The real and imaginary signal paths of the digital time domain compensation module 210 have the same frequency characteristics for removing the distortion which occurs on each of the real and imaginary signal paths due to the group delay variation caused by the analog LPFs 165, 170. Thus, the real and imaginary compensated signals output by real and imaginary compensated signal outputs 260, 270, of the time domain compensation module 210 do not include the distortion.

[0038] Figure 3 shows a plurality of successively connected real delay (i.e., weighting) units 330_0, 330_1,...,330_{N-2}, 330_{N-1}, are connected in series along the real signal path of the digital time domain compensation module 210 to apply respective delays to a plurality of real filter coefficient unit positions (i.e., tabs) 310_0, 310_1,

310_2,..., 310_{N-2}, 310_{N-1}. For example, a first active real filter coefficient unit located at the real filter coefficient unit position 310_0 has an input connected to the input of a first real delay unit 330_0. A second real filter coefficient unit position 310_1 is located between the output of the first real delay unit 330_0 and the input of a second real delay unit 330_1. As shown in Figure 3, a real filter coefficient unit is not active (i.e., it is passive) at the second real filter coefficient unit position 310_1. Thus, the second real filter coefficient unit position 310_1 does not contribute to the compensation characteristics of the time domain compensation module 210 (i.e., its output is zero).

[0039] A second active real filter coefficient unit located at the third real filter coefficient unit position 310_2 has an input connected to the output of the second real delay unit 330_1, and so on, until an active real filter coefficient unit located at the N-2 real filter coefficient unit position 310_{N-2} has an input connected to the output of an N-2 real delay unit 330_{N-2} and to the input of an N-1 real delay unit 330_{N-1}. Finally, an active real filter coefficient unit located at the N-1 real filter coefficient unit position 310_{N-1} has an input connected to the output of the N-1 real delay unit 330_{N-1}. The outputs of each of the active real filter coefficient units are summed at a combiner 320. The combiner 320 applies a real combined compensation signal to the real compensated signal output 260 of the digital time domain compensation module 210, based on the contribution of all of the active filter real coefficient units.

[0040] Furthermore, as shown in Figure 3, a plurality of successively connected imaginary delay units 335_0, 335_1,...,335_{N-2}, 335_{N-1}, are connected in series along the imaginary signal path of the digital time domain compensation module 210 to apply respective delays to a plurality of imaginary filter coefficient unit positions (i.e., tabs) 315_0, 315_1, 315_2,..., 315_{N-2}, 315_{N-1}. For example, a first active imaginary filter coefficient unit located at the imaginary filter coefficient unit position 315_0 has an input connected to the input of a first imaginary delay unit 335_0. A second imaginary filter coefficient unit position 315_1 is located between the output of the first imaginary delay unit 335_0 and the input of a second imaginary delay unit 335_1. As shown in

Figure 3, an imaginary filter coefficient unit is not active (i.e., it is passive) at the second imaginary filter coefficient unit position 315_1. Thus, the second imaginary filter coefficient unit position 315_1 does not contribute to the compensation characteristics of the time domain compensation module 210 (i.e., its output is zero).

[0041] A second active imaginary filter coefficient unit located at the third imaginary filter coefficient unit position 315_2 has an input connected to the output of the second imaginary delay unit 335_1, and so on, until an active imaginary filter coefficient unit located at the N-2 imaginary filter coefficient unit position 315_{N-2} has an input connected to the output of an N-2 imaginary delay unit 335_{N-2} and to the input of an N-1 imaginary delay unit 335_{N-1}. Finally, an active imaginary filter coefficient unit located at the N-1 imaginary filter coefficient unit position 315_{N-1} has an input connected to the output of the N-1 imaginary delay unit 335_{N-1}. The outputs of each of the active imaginary filter coefficient units are summed at a combiner 320. The combiner 320 applies an imaginary combined compensation signal to the imaginary compensated signal output 270 of the digital time domain compensation module 210, based on the contributions of all of the active imaginary coefficient units.

[0042] The performance of the digital time domain compensation module 210 is based on the number of active filter coefficient units and by the design of the filter coefficients associated with each unit of the digital filter therein. The more active filter coefficient units that are incorporated into the digital time domain compensation module 210, the more the digital time domain compensation module 210 will converge toward ideal characteristics. On the other hand, the more active filter coefficient units the digital time domain compensation module 210 has, the more complex the system will be, resulting in more delay in the processing of real and imaginary signal components.

[0043] The performance of the digital time domain compensation module 210 will also rely on the configuration of the real and imaginary active filter coefficient units. The closer that the performance of the digital time domain compensation module 210

approaches the inverse of the frequency domain of the real and imaginary signal components 175, 180, output by the analog LPFs 165, 170, the more efficiently the signal degradation on the real and imaginary signal paths will be suppressed. Since the number of active coefficient units is less than the total number of coefficient unit positions (i.e., the entire length of the filter), the cost and complexity of the configuration used in the digital time domain compensation module 210 may be less complex and thus it may be constructed at a lower cost.

[0044] The present invention allows the design of the digital time domain compensation module 210 to be less complex by taking into the account that the main selectivity filter in the DBB RF receiver 200 will perform an interpolation function. Thus, the spectral shape of the real and imaginary signal components may be restored using a minimum number of active filter coefficient units.

[0045] It should be understood that the compensation of the real and imaginary signal components may be implemented by the digital time domain compensation module 210 at a sample rate substantially higher than the chip rate (e.g., ten times the chip rate).

[0046] While this invention has been particularly shown and described with reference to preferred embodiments, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the scope of the invention described hereinabove.

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